REMARKS

In the Office Action dated December 24, 2002, claims 1-22 and 24-29 were rejected under 35 U.S.C. § 102 over U.S. Patent No. 6,076,139 (Welker); and claims 23 and 30 were rejected under § 103 over Welker.

In the Response to Arguments section on page 2 of the Office Action, there appears to be a misunderstanding regarding what the Applicant stated in the prior Reply to Office Action. The Office Action on page 2 indicated that "Applicant's arguments features two main points," with one of them being that "[t]he collection of Rambus channels 202-208 [disclosed in Welker] is merely one memory bus . . . ." Applicant actually stated the opposite, that the Rambus bus channels 202-208 disclosed in Welker are multiple buses, not one bus. Moreover, in the prior Reply to Office Action, Applicant noted the statement in Welker itself which indicates that "[t]he Rambus channel is a synchronous high speed *bus* . . . ." Welker, 3:37 (emphasis added). This is an explicit statement in Welker, not merely an argument by Applicant, that one Rambus channel constitutes a bus. The four Rambus channels 202, 204, 206 and 208 shown in Figure 2 of Welker therefore constitute four separate and independent buses.

The memory interface 200 of Welker includes four memory interface controllers (MICs) 310, as shown in Figure 3. A key teaching in Welker is that "[e]ach MIC 310 *independently* controls access to its respective memory channel 202-208." Welker, 7:28-31 (emphasis added). In other words, in Welker, one memory controller independently controls access to one memory bus.

This teaching is contrasted to what is recited in claim 1, namely a system that comprises a memory bus and a plurality of memory controllers, with each memory controller to generate memory requests on *the* memory bus. Claim 1 is explicitly clear that each of the plurality of memory controller is able to generate memory requests on the *same* memory bus. In fact, claim 1 further recites that at least two of the plurality of memory controllers are adapted to generate concurrently pending memory requests on *the* memory bus.

Welker does not disclose plural memory controllers on a memory bus as recited in claim 1. Welker recites four separate and *independent* buses (the Rambus channels) and

four separate and *independent* memory controllers to generate memory requests on each respective memory bus. Two MICs 310 as disclosed in Welker are unable to generate memory requests on the same memory bus. For the foregoing reasons, Applicant respectfully submits that Welker does not anticipate claim 1.

Claim 4 depends from claim 1 and is thus allowable for at least the same reasons. Moreover, claim 4 further recites that the memory bus comprises a Rambus channel. In other words, in claim 4, the plurality of memory controllers are able to generate memory requests on the same Rambus channel. This clearly cannot be achieved and is not disclosed by Welker.

Dependent claim 6 depends from claim 1 and is allowable over Welker for at least the same reasons as claim 1. Moreover, claim 6 further recites that the memory bus comprises plural control portions, with each of the control portions associated with corresponding time slot priority schemes. The Office Action pointed to the MICs 310 as being the recited plural control portions. The MICs 310 were cited in the Office Action as being the memory controllers with respect to claim 1. The MICs 310 do not constitute control portions of a memory bus. Examples of control portions of a bus are control signals on the bus. Welker does not disclose the further recited features of claim 6.

Independent claim 10 is also not anticipated by Welker. Claim 10 recites a system having a memory bus and a plurality of memory controllers connected to the memory bus, with each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions. The Office Action stated that the element "each memory controller to monitor memory requests generated by another memory controller" is satisfied by the teaching in Welker that "each MIC controller includes its own snoop controller 706 generating snoop cycles and the return snoop transactions response which the requesting controller acknowledges." 12/24/02 Office Action at 8. Applicant respectfully disagrees. Each MIC 310 in Welker does not monitor memory requests of another MIC 310. The snoop controller 706 within each MIC controller does not monitor memory requests generated by another MIC 310. The snoop controller 706 responds to a request from a bus master (212-220) by generating a snoop request to the central snoop arbiter 312 (Figure 3 of Welker). The central snoop arbiter 312 can receive multiple snoop requests from the MICs 310. The central snoop

arbiter 312 selects one of these snoop requests and forwards it to the processor interface controller 300 (Figure 3) to perform the snoop cycle. Thus, it is clear that the snoop controller within each MIC does not monitor memory requests generated by another MIC. Therefore, independent claim 10 is allowable over Welker.

Independent claims 15 and 23 are allowable over Welker for reasons similar to those given for claim 10.

In view of the foregoing, it is respectfully submitted that the final rejection be withdrawn and the claims be allowed. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 50-1673 (9295).

Respectfully submitted,

2/24/03
Date

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